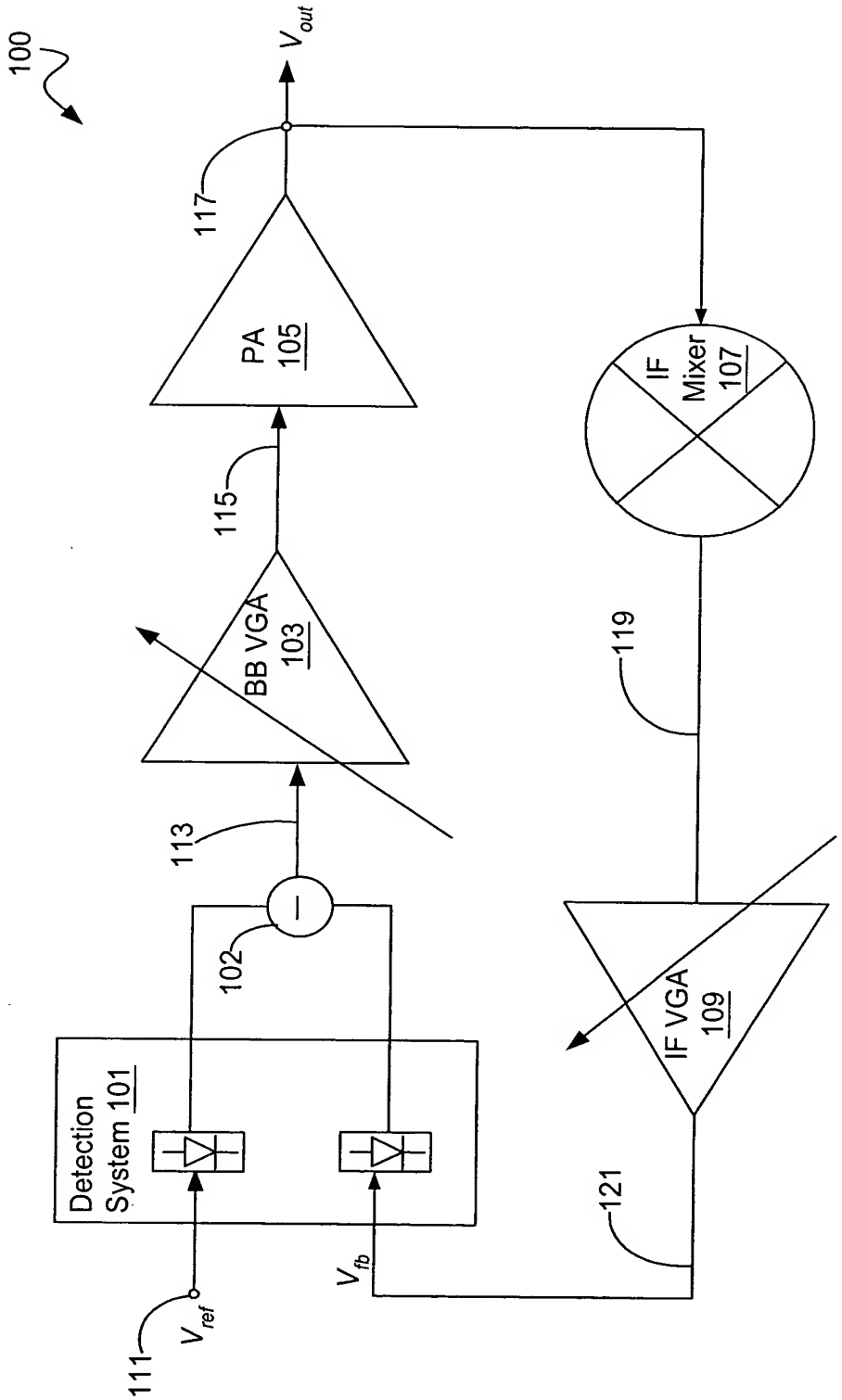


FIG. 1
(Prior Art)

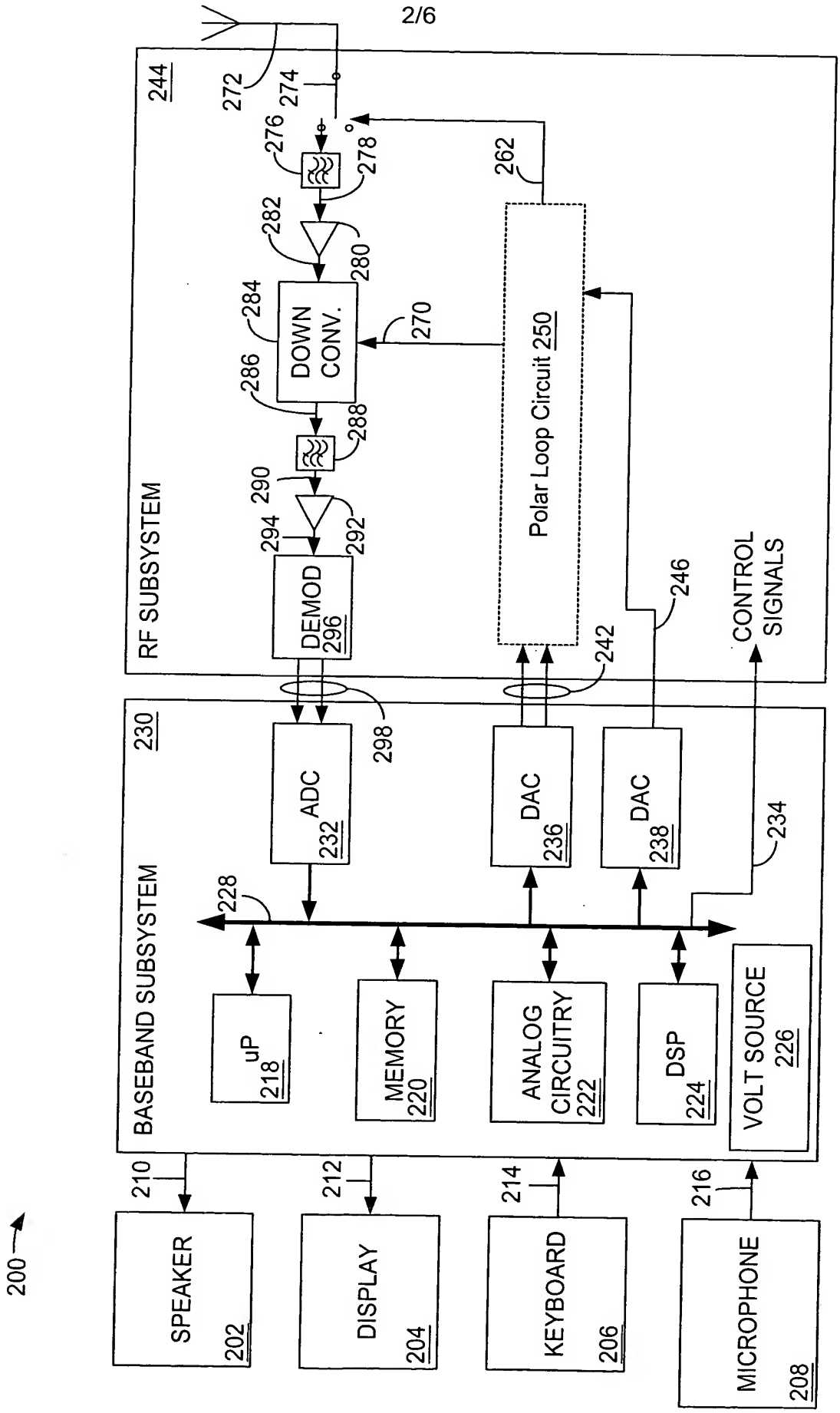
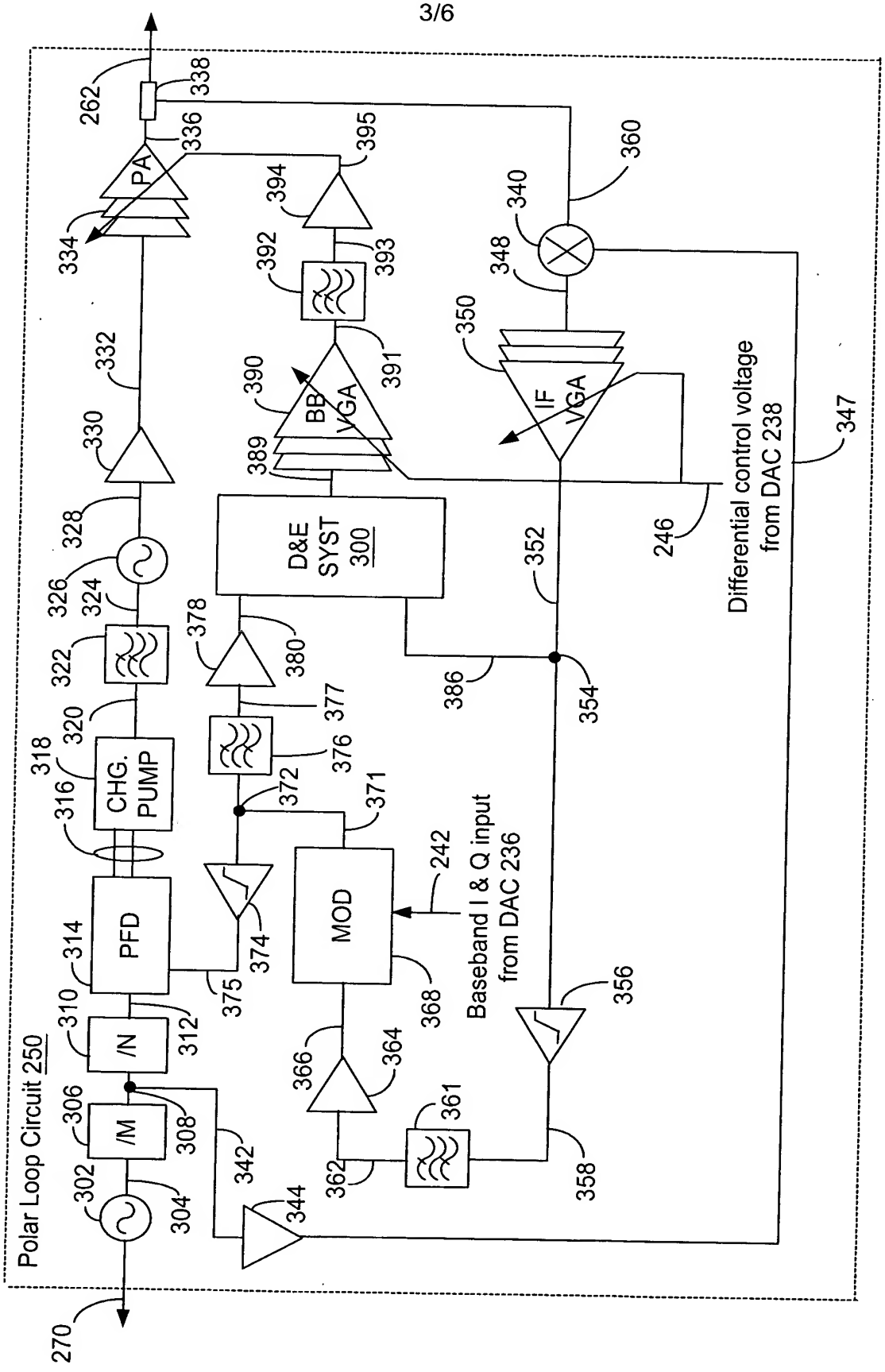

200
SPEAKER 202
DISPLAY 204
KEYBOARD 206
MICROPHONE 208
210
212
214
216
BASEBAND SUBSYSTEM 230
uP 218
MEMORY 220
ANALOG CIRCUITRY 222
DSP 224
VOLT SOURCE 226
228
ADC 232
DAC 236
DAC 238
234
298
242
246
CONTROL SIGNALS
RF SUBSYSTEM 244
DEMOD 296
294
292
290
288
DOWN CONV.
286
284
270
280
282
278
276
274
272
262
Polar Loop Circuit 250

FIG. 2


Polar Loop Circuit 250
PA
/M
/N
PFD
CHG. PUMP
MOD
D&E SYST 300
BB VGA
IF VGA
Baseband I & Q input from DAC 236
Differential control voltage from DAC 238
262
270
302
304
306
308
310
312
314
316
318
320
322
324
326
328
330
332
334
336
338
340
342
344
347
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242
246

FIG. 3

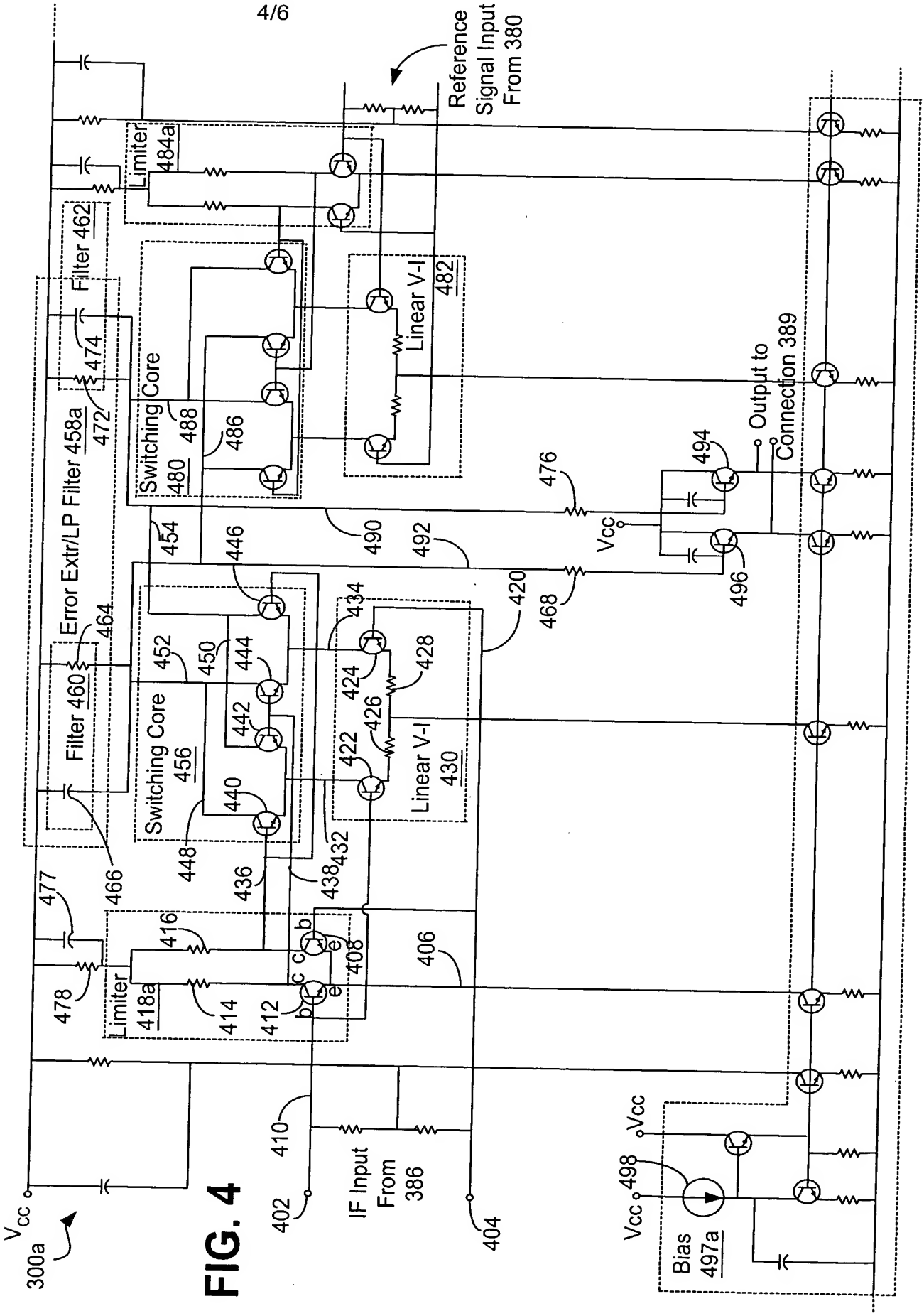

Reference Signal Input From 380
Limiter 484a
Filter 462
474
472
Error Extr/LP Filter 458a
Switching Core 480
488
486
Linear V-I 482
Output to Connection 389
494
476
Vcc
490
492
496
454
446
420
468
464
Filter 460
452
450
444
434
424
428
Switching Core 456
442
426
422
Linear V-I 430
440
448
436
438
432
477
466
416
408
406
478
Limiter 418a
414
412
410
402
IF Input From 386
404
Vcc
498
Bias 497a
300a

FIG. 4

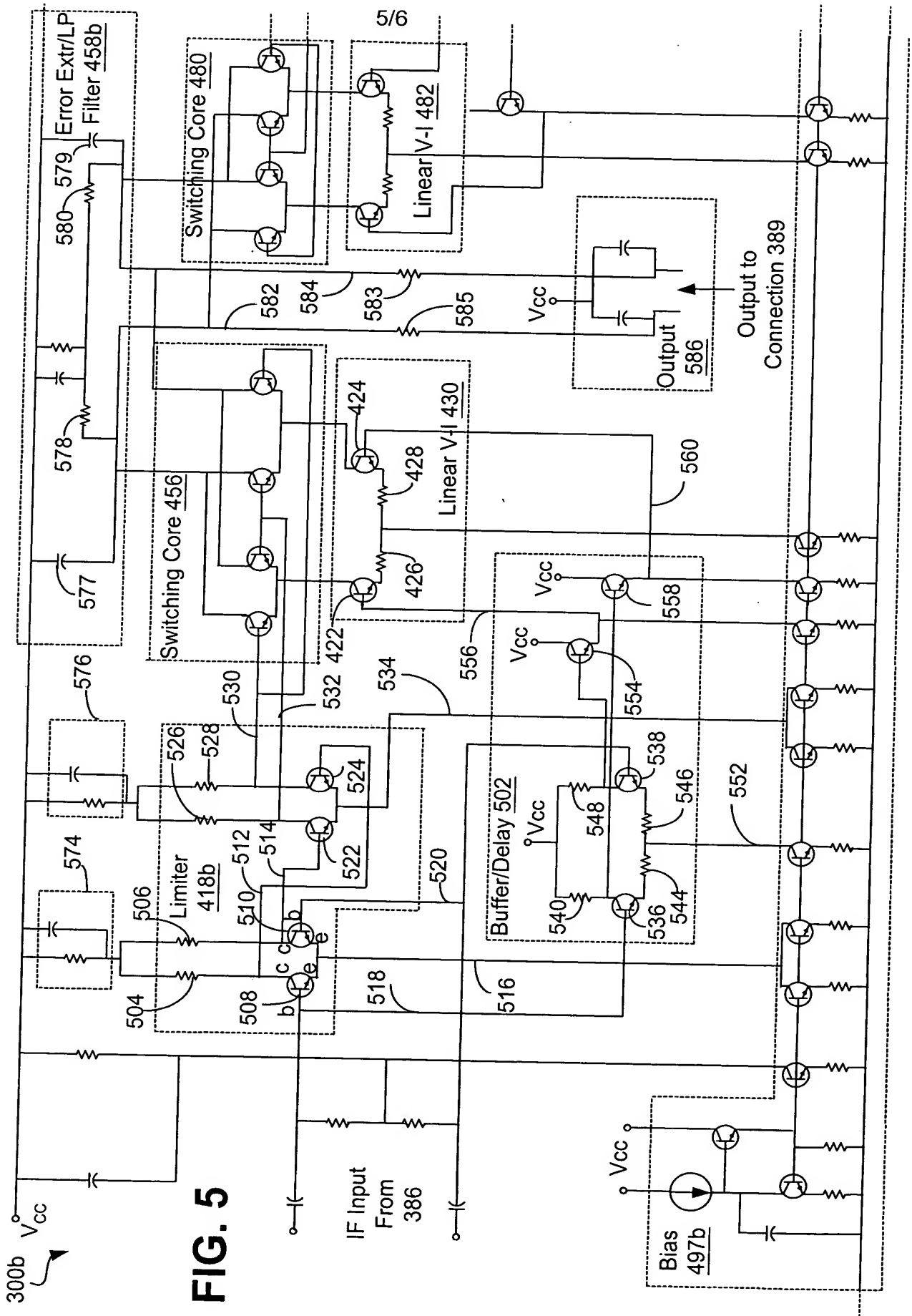
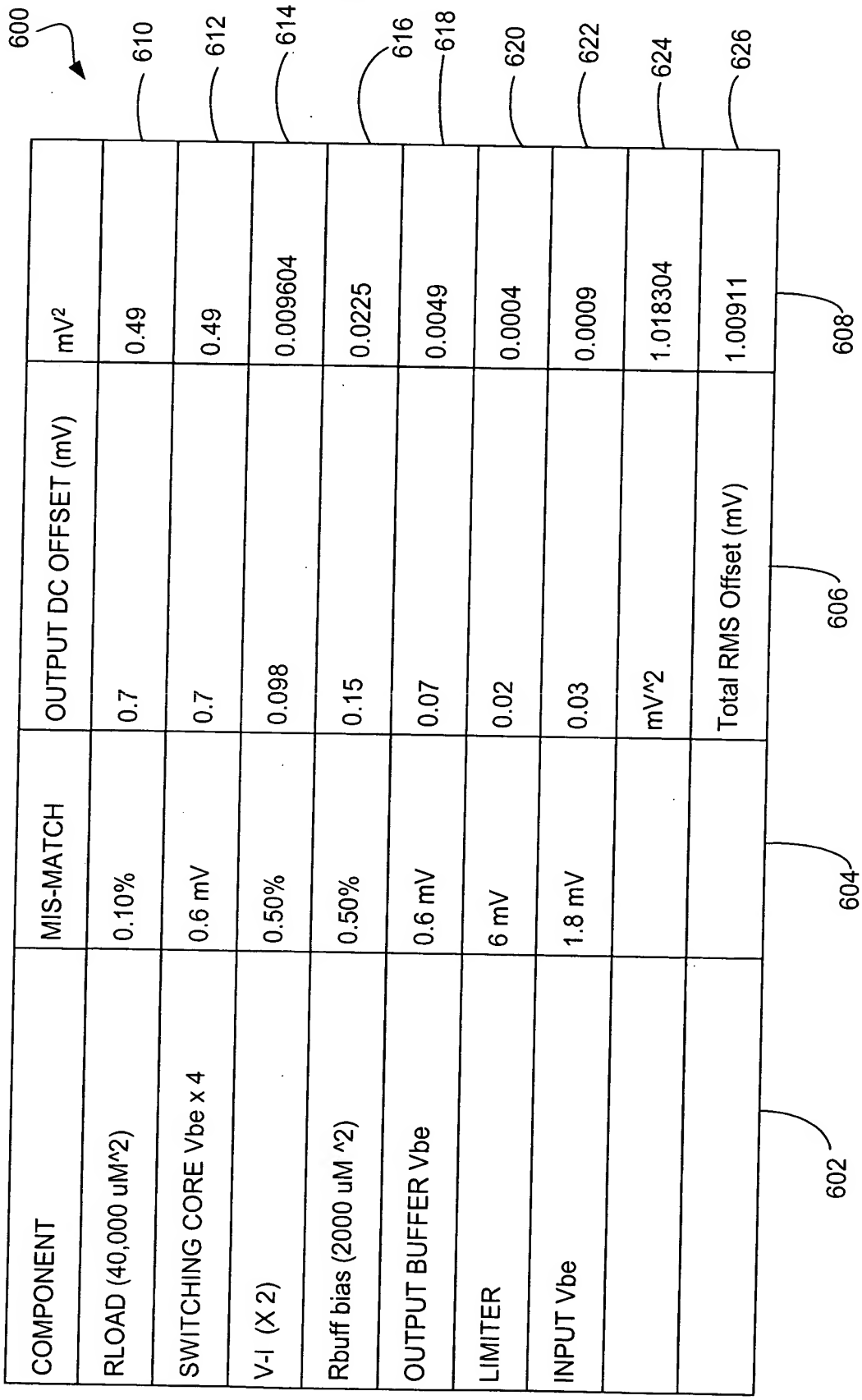

Error Extr/LP Filter 458b
579
580
Switching Core 480
Linear V-I 482
582
584
583
585
Vcc
Output 586
Output to Connection 389
578
424
428
Linear V-I 430
560
Switching Core 456
426
422
577
576
530
532
534
556
Vcc
558
554
526
528
524
538
546
552
548
Buffer/Delay 502
574
512
514
522
520
506
Limiter 418b
510
540
536
544
504
508
518
516
IF Input From 386
Bias 497b
300b
Vcc

FIG. 5



COMPONENT	MIS-MATCH	OUTPUT DC OFFSET (mV)	mV^2
RLOAD (40,000 uM^2)	0.10%	0.7	0.49
SWITCHING CORE Vbe x 4	0.6 mV	0.7	0.49
V-I (X 2)	0.50%	0.098	0.009604
Rbuff bias (2000 uM ^2)	0.50%	0.15	0.0225
OUTPUT BUFFER Vbe	0.6 mV	0.07	0.0049
LIMITER	6 mV	0.02	0.0004
INPUT Vbe	1.8 mV	0.03	0.0009
		mV^2	1.018304
		Total RMS Offset (mV)	1.00911

FIG. 6